

EFFECT OF VOIDS ON THERMO-MECHANICAL RELIABILITY OF SOLDER JOINTS

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ABSTRACT

Despite being a continuous subject of discussion, the existence of voids and their effect on solder joint reliability has always been controversial. In this work we revisit previous works on the various types of voids, their origins and their effect on thermo-mechanical properties of solder joints. We focus on macro voids, intermetallics micro voids, and shrinkage voids, which result from solder paste and alloy characteristics. We compare results from the literature to our own experimental data, and use fatigue-crack initiation and propagation theory to support our findings. Through a series of examples, we show that size and location of macro voids are not the primary factor affecting solder joint mechanical and thermal fatigue life. Indeed, we observe that when these voids area conforms to the IPC-A-610 (D or F) or IPC-7095A standards, macro voids do not have any significant effect on thermal cycling or drop shock performance.

Key words: voids, crack initiation and growth, thermo-mechanical reliability, lead-free.

INTRODUCTION

Since the introduction of near eutectic lead-free alloys in the early 2000's, there was a concern on increased number of voids during the reflow process when compared to eutectic Sn-Pb solder. There have been numerous studies on this subject, including several industry consortiums and standards development dedicated to address this issue [1-3]. Whereas some believe that voids will act as stress concentrators, reducing the solder joint fatigue life, others suppose exactly the opposite, that voids can act as stress relief to reduce the speed of crack propagation. Failures of electronic components undergoing thermal cycling occur due to thermal stresses in solder joints. Depending on the mechanical reliability of these solder joints, these thermal stresses can somehow reduce the solder joint fatigue life.

Prior to starting any further discussion on voids, it is important to distinguish the various types of voids. Some voids result from very specific choices of solder alloys or materials used in the printed circuit board (PCB) design, whereas others are inherent to the surface mount technology

(SMT) process. However, no discussion would be complete without further investigation on how fracture mechanics theories could support (or not) voids as points of stress for crack initiation and growth. Therefore, we start this work by reviewing the related literature and discussing these two topics in more details.

One of the early studies trying to understand the effect of voids on BGA/CSP solder joints fatigue life concluded on some sort of relation between voids and lower thermal cycling performance [4]. In another early study based on finite element method analysis, equivalent plastic strain and shear strain of solder joints with voids of various sizes at different positions were calculated [5]. It concluded that presence of voids does not always have a negative effect on thermal fatigue of the solder joints. Later on, several other experimental and theoretical studies made similar suggestions that thermal fatigue is mostly not affected by the amount of voids in the solder joint. Some of these studies are also reviewed here when discussing the relationships between voids and the solder joint thermal and mechanical reliability.

Failures in electronic components during thermal cycling occur due to thermal stresses in solder joints. These thermal stresses can reduce the solder joint fatigue life, depending on the mechanical reliability of these solder joints. Thus, we compare thermal cycling or drop shock performance of individual solder joints with their respective cross-section appearance. We present various examples taken from our work on Sn-Ag-Cu Pb-free alloys, in which the voids conform to the IPC-A-610 standard (revisions D or F) and reflect actual processing conditions, and compare with the findings in the literature. Finally, we discuss how our experimental data can be viewed in light of fracture mechanics theory for crack initiation and growth.

VOIDS AND CRACKS

Very good descriptions of the various types of voids can be found in the literature, such as the references cited here [6-9]. Basically, voids can be divided in six categories:

- i) Macro Voids: Very common type of voids as they are generated, mostly, by the evolution of volatiles

from the paste flux during reflow. Also known as process voids.

- ii) Intermetallics (IMC) Micro Voids or Kirkendall Voids: Located between the intermetallic layer and the copper substrate. Caused by differences in diffusion rates between Cu and Sn.
- iii) Shrinkage Voids: Unique to Pb-free alloys, these are caused by contraction stresses on solidifying interdendritic eutectic solder.
- iv) Planar Micro Voids: Also called “champagne” voids, are generally smaller than 25 μm . Can occur during various steps in surface finish plating.
- v) Micro-via Voids: Not unique to Pb-free alloys. Caused by micro-vias in the land.
- vi) Pinhole voids: Caused by improper copper plating. Located in the PCB land, generally have 1-3 μm in diameter.

Figure 1 shows a comprehensive summary by Aspandiar [6] describing the types of voids.

The first three categories (macro voids, IMC micro voids, and shrinkage voids) refer to voids resulting from solder paste and alloy characteristics, whereas the last three categories (planar micro voids, micro-via voids, and pinhole voids) occur due to materials used in the PCB or its design.


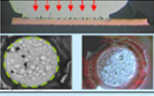

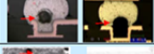


Type of Voids	Description	Photos
Macro Voids	Voids generated by the evolution of volatile ingredients of the fluxes within the solder paste; typically 4 to 12 mils (100 to 300 μm) in diameter; these are usually found anywhere in the solder joint; IPC's 25% max area spec requirement is targeted toward process voids; NOT unique to LF solder joints. Sometimes referred to as “Process” voids	
Planar Micro Voids	Voids smaller than 1 mil (25 μm) in diameter, generally found at the solder to land interfaces in one plane; though recent occurrence on Immersion Silver surface finish has been highlighted these voids are also seen on ENIG and OSP surface finishes; cause is believed to be due to anomalies in the surface finish application process but root cause has not been unequivocally determined. Also called “champagne” voids	
Shrinkage Voids	Though not technically voids, these are linear cracks, with rough, “dendritic” edges emanating from the surface of the solder joints; caused by the solidification sequence of SAC solders and hence, unique to LF solder joints; also called sink holes and hot tears	
Micro-Via Voids	4 mil (100 μm) and more in diameter caused by microvias in lands; these voids are excluded from 25% by area IPC spec; NOT unique to LF solder joints	
Pinhole Voids	Micron sized voids located in the copper of PCB lands but also visible through the surface finish; Generated by excursions in the copper plating process at the board suppliers	
Kirkendall Voids	Sub-micron voids located between the IMC and the Copper Land; Growth occurs at High Temperatures; Caused by Difference in inter-diffusion rate between Cu and Sn. Also Known as “Horsting” Voids.	

Figure 1. Types of voids in solder joints. Reprinted from Ref. [6], with permission of the author.

Macro voids, IMC micro voids, and shrinkage voids can be minimized by adjusting process parameters, alloy composition and paste flux formulation. Macro voids, which are also called process voids, are the most common type of voids in SMT processing and can be minimized by adjusting reflow parameters such as peak temperature, time above liquidus temperature (TAL), and pre-heating time. Shrinkage voids and IMC micro voids can be minimized by using faster cooling rates and optimizing the alloy composition (removal of contaminants), and by using alloying additions, respectively.

It is very important to understand the effect of voids on the solder joint. It is well-known that voids can lead to poor

heat transfer between die and heat sink, and in the worst case cause failures due to thermal stresses. Such risks are generally addressed through design adjustments that compensate for that. The effect of voids on the fatigue life of solder joints though, is still under debate. Before discussing this effect in more details, let us briefly review the mechanisms of crack nucleation and propagation and how they could be affected by voids in the solder joints.

When an alloy is subjected to mechanical stresses it first deforms within the elastic region (up to its yield strength) and later within the plastic region. Elastic deformation can be recovered, whereas plastic deformation is permanent. On a microscopic level, plastic deformation is a result of dislocation movement (primary) or twinning. Fatigue failures in a solder joint occur due to cyclic stresses within the plastic deformation region of an alloy, but below its ultimate tensile strength. Failures through fatigue involve crack initiation, crack propagation and sudden fast failure.

There are distinct causes for crack initiation and crack propagation, which occur due to different mechanisms [10-12]. Cracks mostly originate at a point of stress concentration (e.g., sharp corners, micro cracks, scratches, notches) on the surface. Cyclic straining of the material results in persistent slip bands (movement and accumulation of dislocations), causing the roughening of the surface due to irreversible shear displacement. This roughening is visible as intrusions and extrusions, which end up amplifying local stresses initiating the cracks. Another type of crack initiation in ductile materials occurs through nucleation, growth and coalescence of micro cracks or micro voids under very large deformations. However, this later mechanism does not apply to thermal stresses generated under cyclic expansion and contraction during thermal cycling of solder joints, in which deformations are much smaller.

In general, stronger materials perform better in resisting crack initiation, but crack propagation will depend on the plastic zone ahead of the crack tip (stage I). Thereby, crack propagation depends on the alloy microstructure. Energy is stored in the material during elastic deformation and released during crack propagation as the creation of new surfaces requires energy. As per Griffith's criterion, crack propagation occurs when the released elastic energy is at least equal to the energy required to generate new crack surfaces [12]. In ductile materials the near tip plasticity “blunts” the crack, making harder for it to propagate. Irwin and Orowan modified Griffith's criterion such the critical stress for crack propagation is at least equal to the sum of surface energy to create new crack surfaces and plastic deformation energy. Stage II corresponds to a stable crack growth, in which the microstructure has less influence on the crack growth. Competing mechanisms promoting crack growth and closure are still under debate, but most agree that small changes in the path of the crack, interception of precipitates, roughness or plasticity induced can lead to crack closure, consequently stopping its growth [11].

SOLDER ALLOY/PASTE SELECTION AND VOIDS

From the brief overview on fracture mechanics shown above, in ideal conditions the existence of voids in the solder joint would not directly affect initiation and propagation of cracks resulting from thermal stresses. However, in less than ideal conditions there could be additional factors leading voids to contribute to crack initiation and growth. Some of these voids are related to solder paste and/or alloy and, as such, can be reduced or eliminated by adjusting the composition of these materials. In the present work we will limit our discussions to these three types of voids: (1) macro voids, (2) shrinkage voids, and (3) IMC micro voids, which are illustrated in Figure 2a. Indeed, the relationship between macro voids and crack initiation/ propagation (if any) is of particular interest, since most voids measurements and analysis refer to them. Figure 2b shows that macro voids can be located close to the IMC, either on the package or the substrate side, or away from the solder/substrate interface. A crack can propagate across the solder joint without interacting with the macro voids or intersecting it. In this case, the crack may continue or stop growing upon its intersection with the macro void.

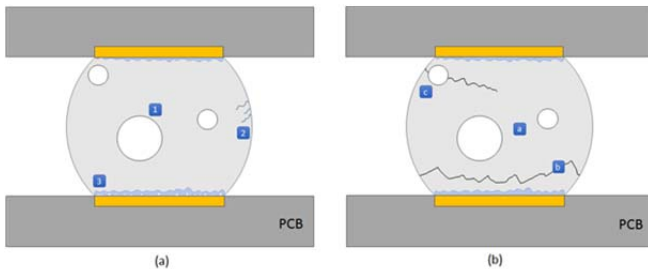


Figure 2. (a) Types of voids related to solder paste and alloy. (b) Relationship between macro voids and crack initiation/propagation.

Shrinkage voids result from contraction during solidification of the molten solder [5-6]. Cooling of eutectic Sn-3.5Ag-0.9Cu, results in sequential solidification of α , $\alpha+\beta$, and $\alpha+\beta+\gamma$ phases, i.e., (Sn), (Sn) + Ag_3Sn , and (Sn) + Ag_3Sn + Cu_6Sn_5 , respectively [13]. Similarly, in other near eutectic Sn-Ag-Cu alloys (e.g., SAC305), all three phases will coexist after complete solidification, but contraction of Sn rich dendrites can result in elongated voids, as shown in the example of Figure 3. Shrinkage voids are mostly located close to the surface and in the bulk of the solder joint, away from the intermetallics region. Despite their resemblance to cracks, this type of voids has little or no effect on solder joint reliability, and can be minimized by adjusting the reflow profile towards a faster cooling rate [6].

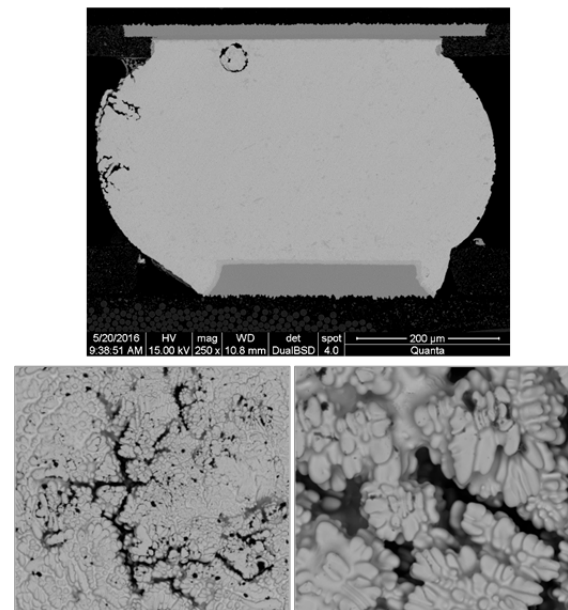


Figure 3. Example of shrinkage voids in Pb-free alloy.

IMC micro voids are found in or on the IMC/Cu interface, between the solder and copper pads. There are multiple accounts of IMC micro voids appearance upon exposure to high temperatures for a certain period of time, including thermal cycling test [14-16]. Despite some controversy, it is generally believed that these IMC micro voids are a result of the Kirkendall effect, so they are also commonly called Kirkendall voids. The Kirkendall effect describes the atomic movement when two metals with different diffusion rates diffuse into each other, demonstrating a vacancy diffusion. This type of voids can occur in solder joints using both Sn-Pb and Pb-free alloys, as they result from Cu diffusing faster than Sn. Figure 4 illustrates the mechanism of formation of Kirkendall voids in solder joints [16]. Copper atoms diffuse from the pads toward the solder, forming Cu_6Sn_5 intermetallics, which are in thermodynamic equilibrium with the Sn from the solder. As the solder loses contact with the Cu pads, solid state reactions occur and, as Cu and Cu_6Sn_5 are not in equilibrium, Cu_3Sn intermetallics is formed in between. As copper continues its diffusion, Kirkendall voids are left at the $\text{Cu}_3\text{Sn}/\text{Cu}$ interface. In addition to that, some Sn from Cu_6Sn_5 also diffuses to the $\text{Cu}_3\text{Sn}/\text{Cu}$ interface, forming Kirkendall voids in the Cu_3Sn intermetallics. Upon extended exposure at temperatures as low as 100°C [15], solid state diffusion will continue the process above, increasing the number of Kirkendall voids.

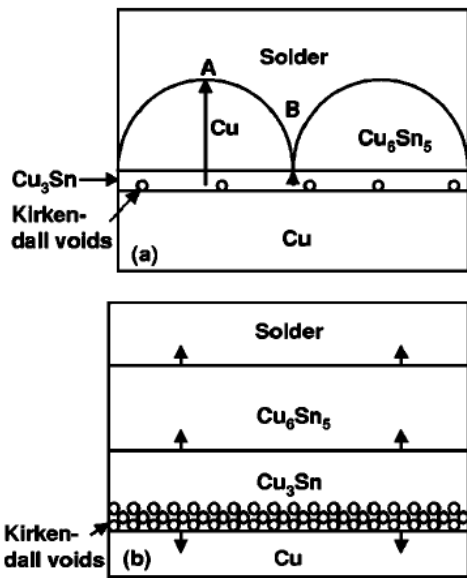


Figure 4. Schematics of how microstructure between solder and copper evolves from (a) as soldered to (b) prolonged exposure to high temperature. Reprinted from Ref. [16], with the permission of AIP Publishing.

Experimental data showed that the number of IMC micro voids grows during thermal cycling test. Mathematical models have explored this phenomenon further, observing a sort of Ostwald ripening, in which the fraction of large voids grows at the expense of small voids [17]. Figure 5 shows examples of IMC micro voids growth under storage at constant 175°C. In the Sn-4Ag-0.5Cu solder, IMC micro voids are visible in the Cu_3Sn layer, after as early as 100 h storage (Figure 5a). The number of IMC micro voids grows with the extended exposure under high temperature. However, their number is comparatively less in Sn-0.3Ag-0.7Cu-X, which can be attributed to its minor alloying additions that are used for controlling Cu_6Sn_5 and Cu_3Sn growth, as showed in Table 1.

Although IMC micro voids will not initiate cracks, they can have a significant effect on the mechanical reliability of solder joints as they are mostly located at the $\text{Cu}_3\text{Sn}/\text{Cu}$ interface and may act as stress concentrators for crack growth. For example, Chiu and collaborators [15] have found a strong correlation between the increase in Kirkendall voids during aging and the reduction in drop shock reliability of BGA with Sn-Ag-Cu solder balls. However, various detailed studies demonstrated that the risk posed by Kirkendall voids can be reduced by using alloying additions (e.g., Cu and Ni) to control solder/Cu interfacial diffusion, and consequently, reducing mechanical reliability degradation of solder joints [18-19].

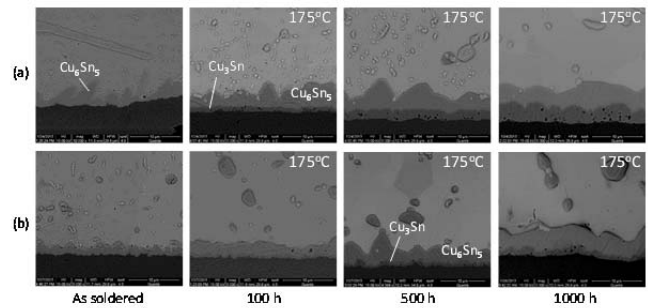


Figure 5. Evolution of IMC micro voids upon aging at 175°C for (a) Sn-4Ag-0.5Cu, and (b) Sn-0.3Ag-0.7Cu-X.

Table 1. Intermetallics thickness of Sn-4Ag-0.5Cu and Sn-0.3Ag-0.7Cu-X after aging.

Condition	IMC thickness, μm	
	Alloy	
Sn-4Ag-0.5Cu		
As soldered	Cu_6Sn_5	Cu_3Sn
100 h	3.15	0
500 h	3.79	0.92
1000 h	3.69	1.87
Sn-0.3Ag-0.7Cu-X		
As soldered	2.03	0
100 h	2.45	0
500 h	3.49	0.84
1000 h	4.85	1.20

Macro voids are generated mostly from the evolution of volatile materials present in the solder paste. A solder paste is a blend of solder powder and paste flux in proportions around 90-10 wt.% or 50-50 vol.%. The paste flux is composed of rosins/resins, solvents, activators and rheology modifiers. Components with boiling point below the peak reflow temperature will vaporize during reflow, forming bubbles that will move upwards as the alloy particles melt. Most volatiles escape from the solder joint, but few remain entrapped and upon solidification will become macro voids. There has been some indication that macro voids higher incidence in Sn-Ag-Cu alloys is also due to their relatively higher surface tension, when compared to eutectic Sn-Pb [20]. Because of their nature and size, most of the concerns about voids in the electronics industry are related to macro voids.

RELATION BETWEEN SOLDER JOINT THERMAL/ MECHANICAL RELIABILITY AND VOIDS

From what we have discussed so far, voids alone do not seem responsible for any reduction of mechanical or thermal fatigue life of solder joints. Next we look how well the experimental evidence matches these findings. From the literature, several studies showed that voids located within the crack propagation path will have a negative effect on the mechanical reliability of the solder joint, otherwise they do not. In one of such studies, Sethuraman and collaborators studied the relationship between macro voids and fatigue life of Sn-37Pb 84 I/O CSP on Electrolytic Ni/Au [21]. In

their study, high densities of voids were intentionally created for impacting fatigue life of solder joints. They confirmed a hypothesis of a void-assisted failure mechanism, in which size and location (on the crack propagation path) of macro voids affect solder joint fatigue life. In another study, Coyle and collaborators [22] investigated effect of voids on the fatigue life of larger packages, 680 I/O PBGA with SAC305 solder ball/solder paste. Their experimental data corroborated prior studies, showing that voids can reduce the solder joint fatigue life “only when the voids were located in proximity to the eventual propagation path of the fatigue crack”. Both studies evaluated fatigue failure due to thermal cycling test from 0 to 100°C, with 10 min dwells and heating/cooling ramps.

More recently, Hillman and collaborators [23] verified similar behaviour of solder joints exposed to thermal cycling conditions typical of higher reliability solder joints, from -40°C to 125°C (15 min dwells and 10 min ramps). They evaluated BGA components with various sizes and pitches and observed that thermal fatigue life of BGAs with voids and without voids was statically the same, but that individual components could be influenced by voids size and location. From this study, they also proposed that voids with area below 20% require no action, whereas voids above 35% area (25% if a corner joint) are not acceptable.

Figure 6 shows metallographic cross-sections of critical joints in BGAs using Sn-37Pb solder paste and ball. Both components showed similar fatigue life, having failed just 100 cycles apart during a thermal cycling test from 0 to 100°C (10 min dwells and ramps). The failure mode in these samples is clear, with cracks on the package side that initiated close to the IMC and propagated through the bulk solder. Interesting to note that the 100 µm macro void on sample (b) is located next to the IMC, but it did not affect the thermal cycling life of the sample. Based on the experimental evidence discussed above, since the macro void is not on the crack propagating path it did not affect the solder joint fatigue life.

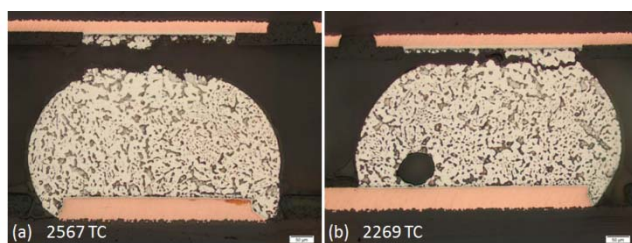


Figure 6. Effect of thermal cycling and voids on Sn-37Pb solder joints.

Figure 7 shows yet another example, of BGAs using Sn-Ag-Cu alloy solder paste and ball, which have been tested in the same thermal cycling profile. Sample (a) exemplifies the failure mode observed for SAC305 samples under this thermal cycling test, in which cracks initiate and propagate through the IMC, either on the PCB or package side. Sample (b) also exemplified the typical failure mode

observed for Sn-Ag-Cu-X samples during this test, in which cracks initiated and propagated through the bulk solder on the package side. These two samples showed the same thermal cycling performance, failing around 4700 cycles, despite the presence of a void in the crack propagation path in sample (b). Sample (c) is one example of a small macro void that is close to the IMC, on the PCB side, but that does not participate at all in the failure of the solder joint as it is completely away from the crack propagation path. Finally, sample (d) is a very good example on how fatigue life depends on the relation between solder joint failure mode and strength/ductility of the material in the crack propagation path rather than on voids. In this case, this component survived only 363 thermal cycles and failed due to cracks initiating and propagating completely through the IMC on the PCB side. Other cross-sections (not showed here) comparing these two alloys showed similar trend, in which the fatigue life depends primarily on the solder alloy and IMC composition rather than on the presence/location of voids.

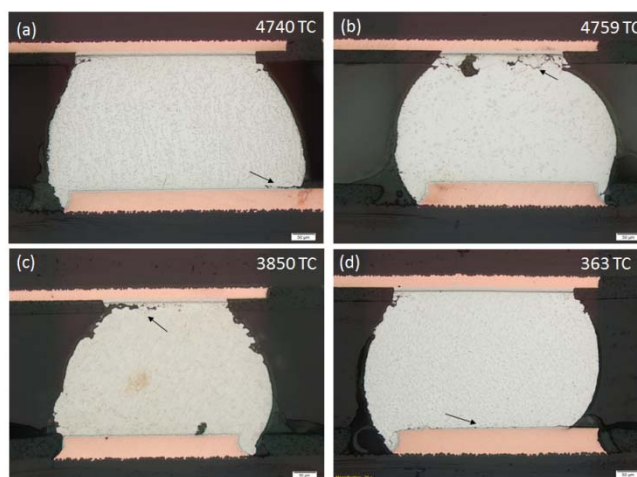


Figure 7. Metallographic cross-sections after thermal cycling test. (a), (d) SAC305, and (b), (c) Sn-Ag-Cu-X. (Arrows indicate cracks).

Although most of the data showed in the literature shows that macro voids have little effect on fatigue life of solder joints, unless the voids are located on the crack propagation path, a similar trend can be showed for samples under shock and vibration. Figure 8 shows metallographic cross-sections of Sn-Ag-Cu-X solder paste/ball after drop shock test. Sample (a) has no macro voids, whereas sample (b) has a void at the PCB side and other smaller voids on the package side. A small crack has intercepted the small voids, but the crack has not progressed into total failure. Solder mask defined pads ensured that crack initiation occurred at the point where the mask intersected the solder, on the PCB side. Despite being located on crack propagation path, the void in sample (b) did not affected the BGA drop shock life (809 drops), which is longer than sample (a) that has no voids (376 drops).

Similarly to previous studies, we have also observed that the amount of voids does not have a direct effect on the thermo-

mechanical reliability of solder joints. For example, Table 2 shows transmission X-ray data of various types of package assembled with SAC305 and another experimental high reliability alloy, called here as alloy A. Except for the CABGA(LGA)144 MD/PD using alloy A, all other solder joints showed voids below 36% of the solder joint area (class 1 as per IPC-7095A). Overall, alloy A shows higher coverage of voids than SAC305. Figure 9 shows Weibull plots of thermal cycling results of these alloys (BGA ball and solder paste), under a -40°C to +150°C profile, using 30 min dwell at the extreme temperatures and 10 min cooling and heating ramps. Despite having higher voids coverage, alloy A has higher characteristic life than SAC305. From this data, we conclude that under these experimental conditions, the amount of voids had no effect on the reduction of fatigue life due to thermal stresses, which is probably more affected by the solder alloy bulk and IMC properties.

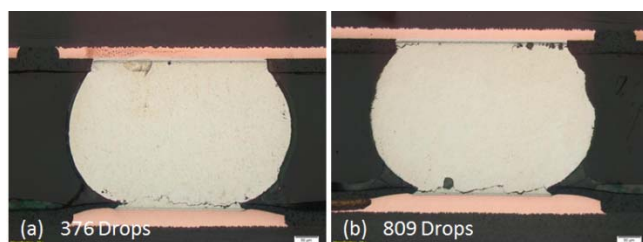


Figure 8. Effect of voids in mechanical reliability drop shock test.

Table 2. Voids measured using transmission X-ray.

Package Type	SAC305		ALLOY A	
	% Voids			
	>9%	>20%	>9%	>20%
BGA208 MD	0	0	22.6	1.4
BGA208 PD	0.48	0	52.2	6.0
BGA256 MD	0	0	2.9	0
BGA256 PD	0	0	8.8	0
CABGA(LGA)144 MD	41.7	3.5	69.1	49.3
CABGA(LGA)144 PD	56.9	9.7	63.8	36.5
PBGA(LGA)144 MD	0.35	0	57.3	3.5
PBGA(LGA)144 PD	0	0	72.9	2.8
PBGA196 MD	0	0	30.1	0.26
PBGA196 PD	0.51	0	60.5	2.5
PBGA208 MD	0.24	0.24	0	0
PBGA208 PD	0	0	1.4	0
PBGA676 MD	0.07	0	0.07	0
PBGA676 PD	0	0	0.22	0

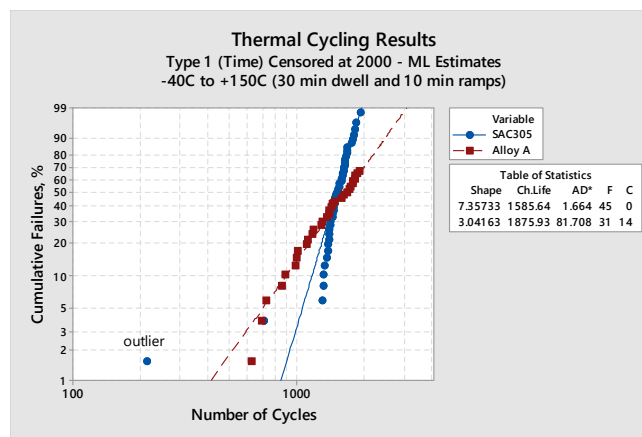


Figure 9. Thermal cycling performance of SAC305 and alloy A.

Thus, in the data showed above we observe that the solder alloy composition is the primary drive behind fatigue life of solder joints. Additionally, when the voids area coverage is below 30%, as per the IPC-A-610F standard, we did not observe any effect of macro voids on thermal cycling or drop shock performance.

Although macro voids are usually controlled by adjusting process parameters, careful formulation of flux chemistry and alloy selection can also help minimizing macro voids [24]. Other alternatives include SMT technologies such as vacuum soldering, which aim to completely eliminate voids from the assembly process. There are advantages and disadvantages of the various vacuum soldering processes, but lower throughput and high capital cost have been the major limitations. Experimental investigations confirmed that applying low pressure vacuum during reflow process significantly reduces the number of voids, which is of especial significance for bottom terminated components [20, 25].

SUMMARY

In the work presented here we have reviewed the types of voids that are frequently found in solder joints, and the mechanisms of crack initiation and growth in metals. Through a series of examples, we discussed in more details the relations between voids resulting from solder paste and alloy characteristics (viz., macro voids, shrinkage voids, and IMC micro voids) and solder joint thermo-mechanical properties. From the literature review and our experimental data, voids located in the bulk of the solder do not affect thermo-mechanical fatigue life of the solder joint. From literature data, IMC micro voids or macro voids located on or close to the IMC may become a concern in case they are located on the crack propagation path. However, our own experimental data shows that when macro voids area is below 30% (as per IPC-A-610F standard), they do not have any significant effect on thermal cycling or drop shock performance.

Although the conclusions showed in this study can be extended to more generic situations, they are still limited to

the experimental conditions and alloys discussed here. For example, under other accelerated thermal cycling conditions, the critical level of voids may be different depending on the fatigue life required. There remains in the industry a strong perception that less voiding is better. Nonetheless, we hope the mechanistic understanding presented here will contribute to the efforts to continue minimizing voiding to meet the demands of the industry.

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